Introduction to the Issue on DSP Techiques for RF/Analog Circuit Impairments

RECENT advances in digital processing capabilities and VLSI integration, fueled by Moore's law, have widened the gap between digital and analog circuits in terms of their performance-complexity tradeoffs. This trend is projected to become even more significant in the future. Radio frequency (RF) impairments in analog circuits are mainly due to fabrication process variations, which are difficult to predict or control, and will continue to increase with fabrication technology down scaling.

Traditionally, wireless transceivers used the super heterodyne architecture where the RF signal is converted down to baseband through one or two intermediate frequency (IF) stages. At each analog IF stage, filtering and amplification are applied to achieve acceptable signal selectivity and sensitivity. The main drawback of this architecture is the large number of analog components (filters and amplifiers) needed to achieve satisfactory signal quality which add to the overall power consumption and cost. To overcome these drawbacks, the direct-conversion architecture (where the RF signal is converted directly to baseband) has gained increased popularity recently since it enables low-cost low-power integration in CMOS technology leading to a smaller form factor. However, direct-conversion broadband wireless transceivers suffer from several major RF/analog impairments which limit their performance. These impairments include I/Q imbalance, phase noise, dc offset, amplifier nonlinearities, just to name a few. Left uncompensated for, these impairments can severely limit the performance, especially at higher carrier frequencies and data rates which is the regime where next-generation broadband wireless systems will operate.

Compensating these RF/Analog impairments in the analog domain is very challenging due to performance–cost considerations. Embedded digital processors and custom ASICS in mobile devices are becoming increasingly more powerful. Furthermore, recently proposed system-on-chip (SoC) architectures bring increased levels of integration putting RF and digital signal processing not only in the same package but integrating them on the same die, thus providing a large amount of bandwidth that used to be limited in multi-die and multi-package solutions. These considerations have spurred recent research activities in the signal processing and circuits technical communities on effective digital baseband compensation techniques for "dirty" RF/analog circuits. **The objective of this inter-disciplinary special issue is to highlight the important role of digital signal processing techniques in understanding and mitigating RF/analog circuit impairments**.

Important progress has been made in the last few years in demonstrating the effectiveness of DSP techniques in modeling and compensating RF/analog impairments. Examples include: techniques to reduce the peak-to-average ratio of OFDM signals and hence clipping distortion in nonlinear amplifiers, adaptive DSP algorithms to compensate for I/Q imbalance in direct-conversion receivers and optimizing overall receiver EVM, ADC, and DAC imperfections (nonlinearities, conversion errors, timing skew), predistortion for nonlinear transmitters and joint channel and frequency offset estimation algorithms, to name a few. However, there are numerous important open problems in this area. One such problem is developing a comprehensive theory and algorithms for digital receiver design under a low-precision "sloppy" analog-to-digital converter (ADC). The high sampling rates used in broadband systems make high-precision ADCs too costly and power hungry. The main theme in these problems is to relax the stringent performance specifications on analog/RF circuits (to reduce fabrication cost) and compensate for the resulting performance degradation in the digital baseband domain which is a much more cost-effective approach. Finally, as analog building blocks are becoming more expensive in smaller process geometries, the use of digital pre- or postprocessing to calibrate and correct, referred to as "digitally assisted analog," has become one of the more active areas in circuit innovation.

The significant performance improvements expected from digital baseband compensation algorithms will directly translate into significant performance gains (in terms of data rate, coverage area, reliability, and battery life) which, in turn, will enhance the overall user experience. The multidisciplinary (signal processing, RF design, communication theory, digital/analog circuits) and multifaceted (theoretical, algorithmic, systems, circuits) nature of this research area will broaden its positive impact to a wide range of problems and applications. Due to the enormous complexity of broadband wireless systems design and implementation, it is no longer enough for an engineer to have an isolated specialty, e.g., communications engineer, DSP engineer, networks engineer, RF engineer, etc. To arrive at an efficient design, all of the involved engineers have to be vertically integrated and understand the implications of their work on other aspects of the design and the overall system. Not everyone has to be an expert in every aspect, but they should have a deep understanding and appreciation of it.

This special issue contains 15 high-quality papers that cover a wide spectrum of topics related to its main theme including compensation of I/Q imbalance in direct-conversion OFDM transceivers, flexible RF front-end realization for multiple standards, nonlinearity compensation for high-power transmit amplifiers and cross-modulation effects in software-defined radios, and calibration of timing skew in time-interleaved ADCs.

We hope you enjoy this special issue!

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