An Adaptive Structure for Sigma Delta Modulation with Improved Dynamic Range

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***Abstract*—This work proposes a novel structure for adaptive sigma delta modulation that leads to considerable improvement in the dynamic range of the modulator. The quantizer step-size is adapted based on estimates of the input signal to the quantizer block rather than on estimates of the input signal to the modulator itself, as is common in current schemes. The proposed structure can be implemented rather directly by means of analog switches. Theoretical and simulation results show considerable improvement in SNR performance, especially for small amplitude signals, over existing adaptive sigma delta modulators.**

I. Introduction

A general structure for Sigma Delta Modulation (SDM) is shown in Figure 1. The analog input signal $x(t)$ is sampled at a rate higher than the Nyquist rate. The sampler is usually preceded by an anti-aliasing (AA) filter. Since the sampling rate is higher than the Nyquist rate, the design of the AA filter is less constrained. Each sampled analog signal $x(n)$ is then converted into a digital signal $y(n)$ with a certain number of bits.

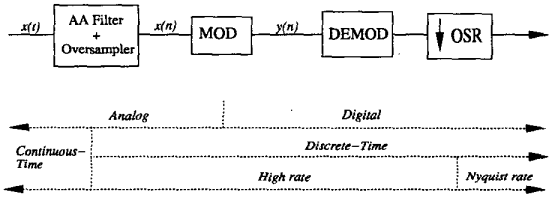

Fig. 1. General structure of sigma delta modulation.

The modulator attempts to shape the noise power spectrum by moving it as much as possible out of the signal band, in order to decrease the in-band noise power. The frequency spectrum of the signal $y(n)$ contains the input signal in its low-band portion. The function of the demodulator is to extract the input signal from the digital sequence $y(n)$, usually by means of a low-pass filter.

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The demodulated signal is still at the high rate and thus needs to be decimated back to the Nyquist rate. Figure 2 shows the modulation/demodulation stages of a single-loop SDM. In this example, the modulator consists of a noise shaping filter $H(z)$ and a single-bit quantizer while the demodulator is a low-pass filter. Other modulator structures include multi-loop, multi-stage, and multi-bit modulators.

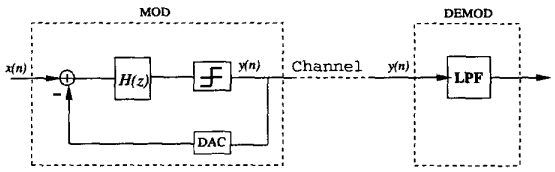

Fig. 2. Modulation/demodulation stages of a single-loop SDM.

Adaptive Sigma Delta Modulation (ASDM) attempts to increase the dynamic range of sigma delta modulators by scaling either the input signal or the step-size of the quantizer through an estimation of the input signal strength. This estimate can be done from the input signal itself or from the modulator output as shown in Figure 3. Input scaling is shown in part a of the figure while step-size scaling is shown in part b. Using the input signal to perform the estimation is known as forward estimation while using the output signal is known as backward estimation. Adaptation could be done continuously or sporadically in time. Moreover, the value of the adaptation signal $d(n)$ could be continuous in amplitude or restricted to a specific range of values.

Several adaptation techniques have been investigated in the literature. Chakravarthy [1] proposed an adaptive scheme that is based on averaging the number of transitions at the modulator output. Jaggi and Chakravarthy [2] used a digital-to-analog converter to instantaneously control the feedback pulse amplitude. Yu et. al. [3] developed a technique based on estimating the maximum input amplitude over a certain interval and using it to adapt the quantization step-size. This work has been extended by Dunn and Sandler [4] to a multi-bit quantizer. Ramesh and Chao [5] implemented a backward adaptation. In their work, the feedback signal of the modulator

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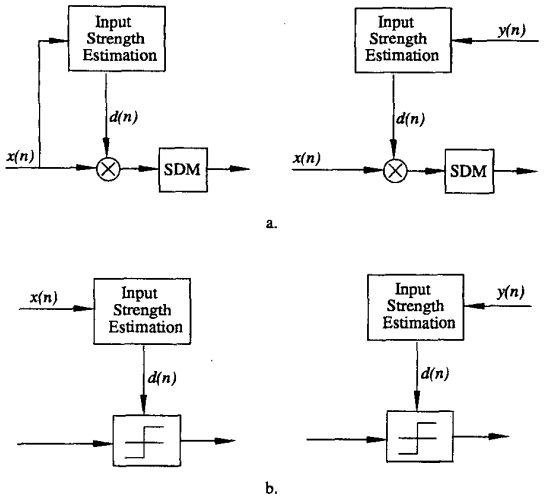

Fig. 3. Adaptation schemes used in conventional ASDM's. a. Input scaling, b. Quantizer step-size scaling.

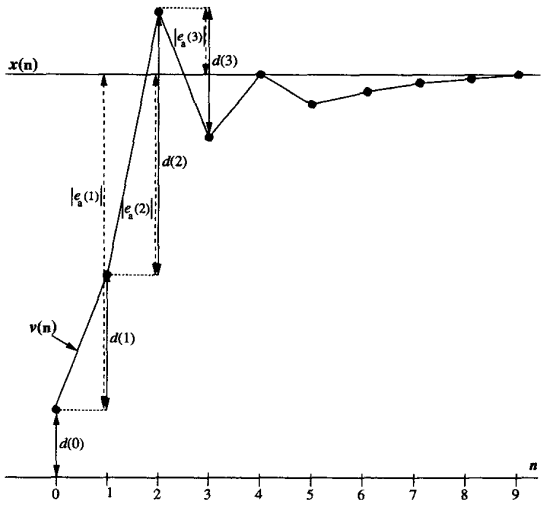

Fig. 4. Response of an output signal $v(n)$ tracking a step input $x(n)$.

is scaled by power-of-two gains based on the estimate of the input amplitude.

In this paper, we develop a different scheme for adapting the quantization step-size. The proposed technique is based on estimating the amplitude of the quantizer input instead of the input signal itself. This estimate is then used to adapt the step size of the quantizer. Theoretical analyses and simulation (here and in [6]) have shown that this structure leads to significant improvement in the dynamic range of the adaptive SDM.

II. New ASDM Structure

A. Motivation

Consider the plot shown in Figure 4. The signal $v(n)$ is tracking a step input signal $x(n)$. The a-priori tracking error at time n is defined by:

$$e_a(n) = x(n) - v(n-1). \tag{1}$$

The signal $v(n)$ is increased or decreased by an amount $d(n)$ depending on the amplitude and the sign of this error. At each iteration, the value of the step $d(n)$ is either doubled or halved. The law by which $d(n)$ varies is chosen to be:

$$d(n) = \begin{cases} 2d(n-1), & \text{if } |e_a(n)| > d(n-1), \\ \frac{1}{2}d(n-1), & \text{otherwise.} \end{cases} \tag{2}$$

Alternatively, we can write

$$d(n) = 2^{w(n)}d(0), \tag{3}$$

where

$$w(n) = w(n-1) + \text{sign}(|e_a(n)| - d(n-1)). \tag{4}$$

The sign of the error $e_a(n)$ decides whether $v(n)$ increases or decreases at each time instance according to

$$v(n) = v(n-1) + \text{sign}(e_a(n))d(n). \tag{5}$$

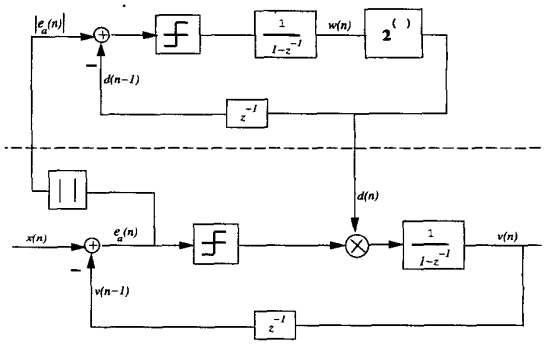

Fig. 5. Adaptive Delta Modulator.

The block diagram shown in Figure 5 is an implementation of the process described above. The top and bottom parts of the figure implement equations (3)-(5). This system belongs to a class of modulation schemes known as Delta Modulation (DM) and more specifically, Adaptive Delta Modulation (ADM). The adaptation technique used here however, is different.

DM is the older version of SDM. The difference is that in delta modulation, no noise shaping is implemented making their performance generally limited. Adaptive DM is adopted to increase the dynamic range of the modulator in a similar way as in ASDM.

B. ASDM Structure

We have seen how the tracking scheme developed in the previous section is implemented in the form of ADM. Since no noise shaping is implemented by ADM, we will extend the design shown in Figure 5 to an ASDM.

Usually, an ADM is converted into ASDM by moving back the integrator of the main loop to become the first block after the adder. Therefore, the basic form of an ASDM is an ADM applied to the integral of the input signal. This process is used to convert the ADM design of the previous section into an ASDM. Higher-order ASDMs can be implemented by replacing the integrator by higher-order noise shaping filters. Furthermore, multi-loop and multi-stage adaptors can be adopted to improve the performance of the modulator.

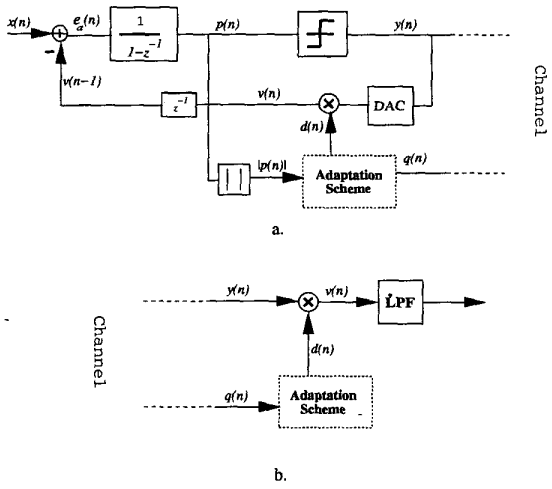

Fig. 6. Block diagram of the proposed structure. a. Modulator b. Demodulator.

Figure 6 shows the basic structure of the proposed adaptive SDM, with a one bit quantizer. The modulation and demodulation blocks are shown in parts a and b, respectively. The error signal $e_a(n)$ is given by

$$e_a(n) = x(n) - v(n-1), \tag{6}$$

which is passed through the noise shaping filter $H(z)$. The filter output $p(n)$ is quantized using a one-bit quantizer to produce the signal $y(n)$. In other words,

$$y(n) = \text{sign}\{p(n)\}. \tag{7}$$

The one-bit DAC is assumed to be ideal and thus has a unity transfer function.

The adapter generates a scaling signal $d(n)$, which is an approximation of the amplitude of the quantizer input signal $p(n)$. The encoded signal $v(n)$ is given by

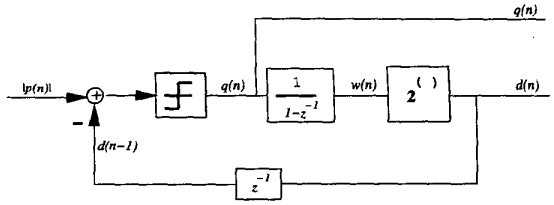

Fig. 7. Adaptation scheme of the proposed modulator.

$$v(n) = y(n)d(n). \tag{8}$$

Note that if $d(n) = |p(n)|$ then we have

$$V(z)/X(z) = 1. \tag{9}$$

The adaptation scheme used in this study (to generate $d(n)$ from $|p(n)|$) is the same as the one used in the ADM case of the previous section (to generate $d(n)$ from $|e_a(n)|$). The adaptor is shown separately in Figure 7. The adaptation block is in itself a delta modulator with an additional exponent term. This additional term boosts the tracking capability of the adapter.

The adaptation signal $d(n)$ is given by

$$d(n) = 2^{q(n)}d(n-1), \tag{10}$$

where the binary sequence $q(n)$ is generated from

$$q(n) = \begin{cases} +1, & \text{if } |p(n)| > d(n-1), \\ -1, & \text{otherwise.} \end{cases} \tag{11}$$

In other words,

$$q(n) = \text{sign}\{|p(n)| - d(n-1)\}. \tag{12}$$

The two binary sequences $y(n)$ and $q(n)$ are carried out to the demodulation part as shown in Figure 6b. There, the signal $v(n)$ is reconstructed using equations (8)-(10). Finally, the reconstructed signal is filtered using a low-pass filter as usually done in conventional sigma delta modulators.

C. Design Considerations

The additional circuitry used in this modulator can be implemented in a simple way using analog switches. The signal $d(n)$ can be generated from equation (10) depending on the state of $q(n)$. Figure 8a shows a block diagram used to generate the signal $d(n)$. The choice between the two gains 2 or $\frac{1}{2}$ depends on the value of $q(n)$ as follows

$$d(n) = \begin{cases} 2d(n-1), & \text{if } q(n) = +1, \\ \frac{1}{2}d(n-1), & \text{if } q(n) = -1. \end{cases} \tag{13}$$

In a similar fashion, the absolute value block in Figure 6 is replaced by a switching device that chooses between

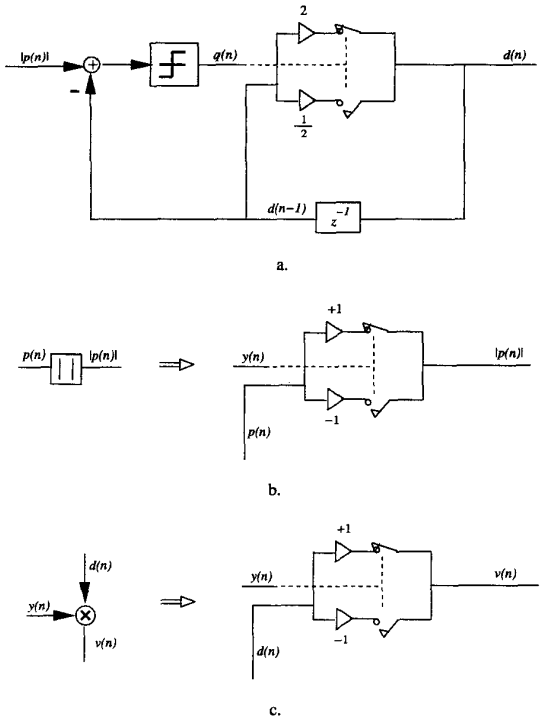

Fig. 8. Implementation of some modulator parts: a) adaptive scheme, b) absolute value term, c) multiplier.

a gain of either $+1$ or -1 depending on the sign of $p(n)$ or equivalently the state of $y(n)$. In other words, the switching system implements the following equation

$$|p(n)| = \begin{cases} +\mathrm{p(n)}, & \text{if } y(n) = +1, \\ -\mathrm{p(n)}, & \text{if } y(n) = -1. \end{cases} \tag{14}$$

This process is depicted in Figure 8b.

Finally, the multiplier in Figure 6 multiplies a real signal $d(n)$ with a binary signal $y(n)$. Thus, it can be replaced by a switch controlled by $y(n)$ to keep or invert the sign of $d(n)$ as shown in Figure 8c i.e.,

$$v(n) = \begin{cases} +\mathrm{d(n)}, & \text{if } y(n) = +1, \\ -\mathrm{d(n)}, & \text{if } y(n) = -1. \end{cases} \tag{15}$$

III. Simulations

The performance of the proposed ASDM has been tested extensively via simulation. The system is simulated using Matlab and Simulink. The input signal used is a sine wave with a frequency of 20KHz. An Oversampling Ratio (OSR) of 128 is used and the initial condition for the adaptation signal $d(0)$ is picked arbitrarily small at 1E-3. The noise shaping filter used is

$$H(z) = \frac{z^2 - 2z + 1}{z^2 - 1.225z + 0.4415}.$$

Figure 9 shows the spectrum of the modulator output $v(n)$ when the input amplitude is -5dB. The amplitude of the input signal is varied and the in-band SNR is measured. The results are plotted in Figure 10 together with the results obtained in [5] for the sake of comparison. The proposed approach clearly demonstrates a superior performance in terms of higher SNR and dynamic range.

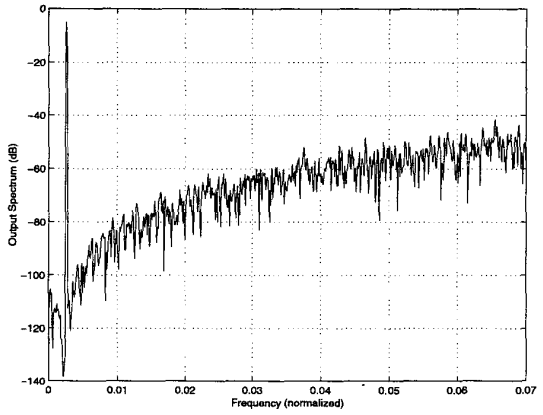

Fig. 9. Spectrum of the modulator output $v(n)$.

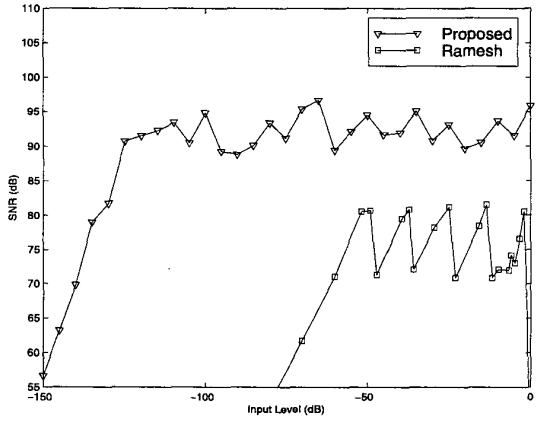

Fig. 10. SNR performance versus input level for the single stage ASDM.

The order of the noise shaping filter $H(z)$ is increased to 4 and 6. In both cases, the SNR performance is measured for the same input. A comparison between the modulator performance for different filter orders is shown in Figure 11. As expected, the modulator shows an improved SNR performance when the order of the filter is increased.

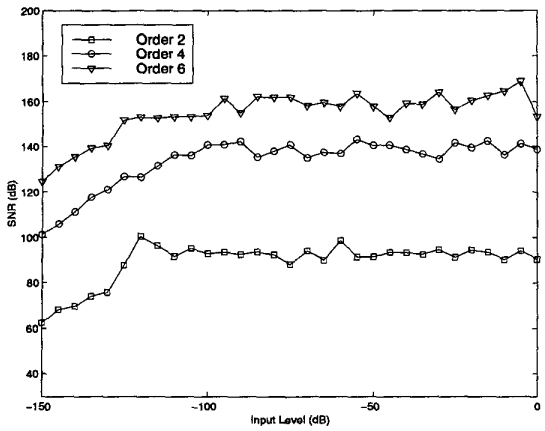

Fig. 11. SNR performance for different orders of the noise shaping filter.

IV. Stability and Performance

In the companion article [6] the performance of the proposed ASDM is studied analytically. In particular, and under some reasonable conditions, the adaptive modulator with a first-order shaping noise filter is proven to be bounded-input bounded-output stable. Moreover, an analytical expression for the SNR of the modulator is derived showing that the SNR is essentially independent of the input signal strength. The expression is further shown to provide a good approximation for the experimental SNR results.

V. Conclusion

A new adaptive sigma delta modulator is proposed. The adaptation scheme is based on approximating the amplitude of the quantizer input rather than the input to the modulator. The adaptation scheme is relatively simple to implement by means of analog switches, and studies have shown that it leads to a high dynamic range performance.

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