Reduction of the Effects of Spurious PLL Tones on A/D Converters

Shang-Kee Ting and Ali H. Sayed
Electrical Engineering Department
University of California, Los Angeles, CA 90095
Email: {tshangke,sayed}@ee.ucla.edu

***Abstract*—In a non-ideal PLL circuit, leakage of the reference signal into the control line produces spurious tones. When the distorted PLL signal is used in an analog-to-digital converter (ADC), it creates spurious tones in the sampled data as well. This paper analyzes this effect and proposes a solution to remove the leakage effects. The algorithm estimates the jitter errors from the spurious sidebands and provides a way to compensate the distorted sampled data in the digital domain.**

***Index Terms*—PLL, sideband suppression, spurious tones**

I. Introduction

In the design of a phase-locked loop (PLL) frequency synthesizer, an important impairment is the presence of spurious tones. The spurious tones result from leakage of the reference signal into the control line of the voltage-controlled oscillator (VCO). Conventional ways to mitigate the problem include improving the linearity of the charged pump and using large capacitors in the loop filter.

Other approaches [1], [2], [3] include increasing the complexity of the circuit design. For example, reference [1] proposed using multiple phase frequency detectors (PFD) and charged pumps that operated in delay with respect to one another. Reference [3] proposed adding another PFD, integrators and voltage-controlled current sources. Moreover, to improve the performance of a fractional-N PLL, reference [2] used a quantizer to replace the delta-sigma modulator that is usually used and added components for charge pump offset and sampled loop filter. These techniques are done mainly in the circuit domain. We propose a different approach to the problem using digital signal processing techniques. The use of digital signal processing to improve performance due to circuit imperfections was used before in addressing IQ imbalances and phase noise in wireless systems [4], [5].

The main motivation for suppressing the spurious tones is that the PLL clock is generally used as the sampling clock in an analog-to-digital (ADC) converter. The spurious tones of the clock introduce spurious sidebands in the sampled data. Rather than reduce the PLL sidebands, this paper proposes a method to estimate the sidebands in a sampled sinusoid training signal and then uses this information to annihilate the effects of the spurious sidebands on the sampled data *in the digital domain*. This is done by estimating the jitter errors caused by the sidebands and using an interpolation scheme to remove the effects.

This work was supported in part by DARPA contract N66001-09-1-2029.

II. Effects of Leakage on Clock Signal

In [6], [7], a voltage-controlled oscillator (VCO) is a circuit that generates a periodic clock signal, $s(t)$, whose frequency is a linear function of a control voltage, V_{cont}. Let the gain of the VCO and its "free running" frequency be denoted by K_{vco} and f_s, respectively. The generated clock signal is described by

$$s(t) = A_s \sin\left(2\pi f_s t + K_{\text{vco}} \int_{-\infty}^{t} V_{\text{cont}} dt\right) \tag{1}$$

To attain some desired oscillation frequency, V_{cont} is set to some constant value. However, the generated signal, $s(t)$, may not be an accurate tone. To attain good frequency synthesis, a down-sampled version of the clock signal is fed into a block that consists of a phase-frequency detector (PFD), a charged pump (CP) and a low-pass filter (LPF) as shown in Figure 1. The PFD/CP/LPF block compares the down-converted frequency clock signal with a low-frequency reference signal at f_{ref} and makes adjustments to V_{cont}. Due to imperfections in the circuitry, the reference signal leaks into the control line of the VCO. For simplicity, we assume that the desired clock signal at f_s is obtained when V_{cont} is 0. Now, suppose there is leakage and V_{cont} is

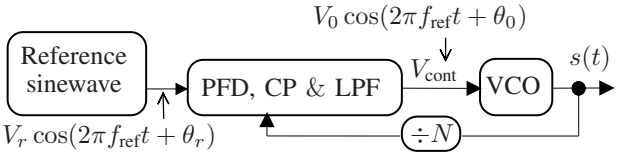

Fig. 1. Block diagram of a PLL

$$V_{\text{cont}} = V_0 \cos(2\pi f_{\text{ref}} t + \theta_0) \tag{2}$$

for some $\{V_0, \theta_0\}$. Then the output of the VCO becomes

$$s(t) = A_s \sin(2\pi f_s t + C_0 \sin(2\pi f_{\text{ref}} t + \theta_0) + \phi_s) \tag{3}$$

where ϕ_s is some unknown phase offset and

$$C_0 = \frac{K_{\text{vco}}}{2\pi f_{\text{ref}}} V_0 \tag{4}$$

We will be analyzing the signal model with respect to an arbitrary reference time. Using a change of variables, let $t = t' - \frac{\phi_s}{2\pi f_s}$, and substitute t into equations (2) and (3).

The new equations are similar to the original equations except that ϕ_s is 0. Therefore, we can let $\phi_s = 0$ without loss of generality. Now the actual sampling instants of an ADC that uses a clock signal of the form of (3) are the zero-crossings of $s(t)$. Using (3) and defining $T_s = 1/f_s$, the sampling instants, t_n, of the ADC must satisfy the condition:

$$2\pi f_s \left(t_n + \frac{C_0}{2\pi f_s} \sin(2\pi f_{\text{ref}} t_n + \theta_0) \right) = 2\pi n \tag{5}$$

Let

$$\begin{aligned} \epsilon_s(n) &= \frac{C_0}{2\pi f_s} \sin(2\pi f_{\text{ref}}\, nT_s + \theta_0) \\ \epsilon_c(n) &= \frac{C_0}{2\pi f_s} \cos(2\pi f_{\text{ref}}\, nT_s + \theta_0) \end{aligned} \tag{6}$$

Some analysis will show that the zero-crossings occur at times $t_n = nT_s + e(n)$, where

$$e(n) \approx -\epsilon_s(n) + 2\pi f_{\text{ref}} \epsilon_s(n)\epsilon_c(n) \tag{7}$$

We omit the derivation for brevity. Let us analyze the effect of this distorted sampling on a pure sinusoidal training tone. Let the input signal to the ADC be

$$w(t) = A_w \cos(2\pi f_w t + \phi_w) \tag{8}$$

Then the sampled signal, $\tilde{w}(n)$, is approximated as

$$\begin{aligned} \tilde{w}(n) &\approx w\left(nT_s - \epsilon_s(n) + 2\pi f_{\text{ref}} \epsilon_s(n)\epsilon_c(n)\right) \\ &= w\left(nT_s + e(n)\right) \\ &\approx w(n) + e(n)\, \dot{w}(n) \end{aligned} \tag{9}$$

where $w(n) = w(t)|_{t=nT_s}$ and $\dot{w}(n) = \dot{w}(t)|_{t=nT_s}$. The term $e(n)\,\dot{w}(n)$ in (9) can be verified to contain 4 frequency components at $f_w \pm f_{\text{ref}}$ and $f_w \pm 2f_{\text{ref}}$. The components are

$$\begin{aligned} \frac{f_w A_w C_0}{2f_s} &[\cos(2\pi(f_w - f_{\text{ref}})nT_s + \phi_w - \theta_0) \\ &- \cos(2\pi(f_w + f_{\text{ref}})nT_s + \phi_w + \theta_0)] \end{aligned} \tag{10}$$

and

$$\begin{aligned} \frac{f_w A_w f_{\text{ref}} (C_0)^2}{4(f_s)^2} &[\cos(2\pi(f_w - 2f_{\text{ref}})nT_s + \phi_w - 2\theta_0) \\ &- \cos(2\pi(f_w + 2f_{\text{ref}})nT_s + \phi_w + 2\theta_0)) \end{aligned} \tag{11}$$

It is observed that the amplitude of the frequencies at $f_w \pm 2f_{\text{ref}}$ is small compared to the frequencies components at $f_w \pm f_{\text{ref}}$ and therefore they can be ignored. Figure 2 shows a realization of the distorted PLL clock at 1GHz and the sampled sinusoidal tone at 40 MHz. The power ratio of the sidebands of the clock, $s(t)$, to the tone at f_s is -50dBc, which induces sidebands in the sampled sinusoidal signal with a power ratio of -78dBc.

We can use the results in (10) to evaluate the sampling offsets' parameters $\{C_0, \theta_0\}$ in (7) and (6) from the sidebands present in $\tilde{w}(n)$. First, we express (8) as

$$w(n) = A_w \cos(2\pi f_w nT_s + \phi_w) \tag{12}$$

Let $Z(f_0) = V_0 e^{j\theta_0}$ denote the complex representation of a sampled sinusoid at frequency f_0 with amplitude V_0 and phase

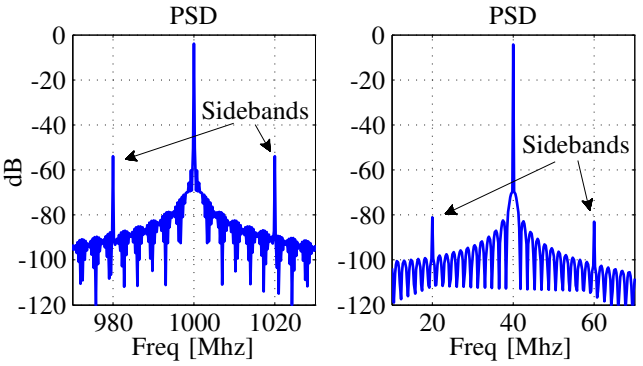

Fig. 2. The left figure shows the PSD of the distorted PLL clock and the right figure shows the PSD of the sampled sinusoidal tone.

θ_0. Then, using (12) and (10), C_0 can be determined from the relation

$$C_0 = B \left| \frac{Z(f_w - f_{\text{ref}})}{Z(f_w)} \right| = B \left| \frac{Z(f_w + f_{\text{ref}})}{Z(f_w)} \right| \tag{13}$$

where

$$B = \frac{2f_s}{f_w}$$

Let * denote complex conjugation. The phase θ_0 can be expressed as

$$\begin{aligned} \theta_0 &= \arg\left[Z(f_w) Z^*(f_w - f_{\text{ref}})\right] \\ &= \arg\left[Z^*(f_w) Z(f_w + f_{\text{ref}}) e^{-i\pi}\right] \end{aligned} \tag{14}$$

The question now is how to estimate the sinusoidal sidebands to enable evaluation of $\{C_0, \theta_0\}$ through (13) and (14). There are various methods to estimate the parameters [8], [9], [10]. One way to estimate the amplitude and phase of a sinusoid at frequency f_k in a signal of the form

$$y(n) = \sum_{k=0}^{K} A_k \cos(2\pi f_k nT_s + \theta_k) \tag{15}$$

is to collect L samples and estimate $\hat{Z}(f_k) = \widehat{A}_k e^{j\hat{\theta}_k}$ using

$$\begin{aligned} \widehat{A}_k &= 2\sqrt{y_c^2 + y_s^2} \\ \hat{\theta}_k &= -\tan^{-1}\left(\frac{y_s}{y_c}\right) \end{aligned} \tag{16}$$

where

$$\begin{aligned} y_c &= \frac{1}{L} \sum_{n=0}^{L-1} y(n)\, \cos(2\pi f_k nT_s) \approx \frac{A_k}{2} \cos(\theta_k) \\ y_s &= \frac{1}{L} \sum_{n=0}^{L-1} y(n)\, \sin(2\pi f_k nT_s) \approx -\frac{A_k}{2} \sin(\theta_k) \end{aligned} \tag{17}$$

From (13) and (14), the parameters in the sampling offsets,

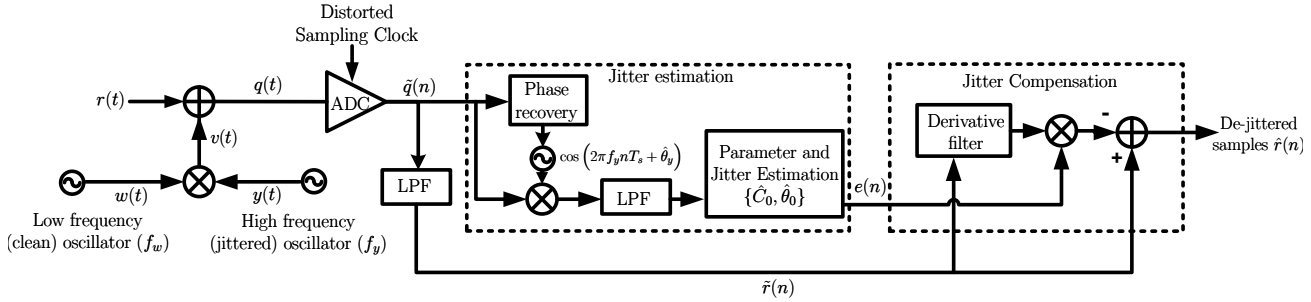

Fig. 3. Proposed architecture for sideband reduction on A/D converters due to spurious PLL tones.

$\{C_0, \theta_0\}$, can then be estimated as follows:

$$\begin{aligned}\hat{C}_0 &= \text{mean}\left\{ B\left|\frac{\hat{Z}(f_w - f_{\text{ref}})}{\hat{Z}(f_w)}\right|, B\left|\frac{\hat{Z}(f_w + f_{ref})}{\hat{Z}(f_w)}\right| \right\} \\ \hat{\theta}_0 &= \text{mean}\Big\{\arg(\hat{Z}(f_w)\hat{Z}^*(f_w - f_{\text{ref}})), \\ &\qquad \arg(\hat{Z}^*(f_w)\hat{Z}(f_w + f_{\text{ref}}))e^{-i\pi}\Big\}\end{aligned} \tag{18}$$

Once $\{C_0, \theta_0\}$ are estimated, we can estimate the jitter errors from (7). In this scenario, the estimated $\hat{Z}(f_w \pm f_{\text{ref}})$ have a larger error because of the strong interfering signal at f_w. To improve the estimation at the sidebands, we can null the interfering signal before estimating the sidebands. This can be done by first estimating $\hat{Z}(f_w)$ from the sampled data, $\tilde{w}(n)$. A digital waveform at frequency f_w with parameters $\hat{Z}(f_w)$ can be created and subtracted from $\tilde{w}(n)$. Finally, the frequency components at $f_w \pm f_{\text{ref}}$ are obtained from the subtracted signal.

III. JITTER SUPPRESSION

We now explain how to modify a technique proposed in [11] in the context of clock jitters in order to remove the jitter effect that is now caused by the PLL sidebands. Figure 3 shows the proposed design. In addition to the input signal, $r(t)$, a low-frequency training signal, $w(t)$, is multiplied with a high-frequency sinusoidal signal, $y(t)$, and added to the ADC input. It is possible that $y(t)$ has some jitter. This operation shifts the training signal to the higher frequency band of the system. We will briefly explain how the clean training signal can be recovered. Define $y(t)$ and its linearized version as:

$$\begin{aligned}y(t) &= \cos(2\pi f_y(t + \tau(t)) + \theta_y) \\ &\approx \cos(2\pi f_y t + \theta_y) - 2\pi f_y \tau(t)\sin(2\pi f_y t + \theta_y)\end{aligned} \tag{19}$$

where $\tau(t)$ is the jitter in $y(t)$ and $\tau(t)$ is assumed to be small. Multiplying $w(t)$ with $y(t)$ yields:

$$\begin{aligned}v(t) &= w(t)y(t) \\ &\approx w(t)(\cos(2\pi f_y t + \theta_y) - 2\pi f_y \tau(t)\sin(2\pi f_y t + \theta_y))\end{aligned} \tag{20}$$

Multiplying $v(t)$ with an in-phase cosine yields:

$$\begin{aligned}v(t)\ \cos(2\pi f_y t + \theta_y) = &\frac{1}{2}w(t)\ (1 + \cos(4\pi f_y t + 2\theta_y) - \\ &2\pi f_y \tau(t)\ \sin(4\pi f_y t + 2\theta_y))\end{aligned} \tag{21}$$

From the above equation, it is observed that $w(t)$ is in the lower frequency band. Therefore, a low-pass filter will remove the higher frequency terms, including the jitter term $\tau(t)$. This idea can be extended to the case where the sampled data, $\tilde{q}(n)$, contains both the modulated training signal, $\tilde{w}(n)\tilde{y}(n)$, and the input signal, $\tilde{r}(n)$. Multiplying $\tilde{q}(n)$ by an in-phase cosine and applying a low-pass filter yields $\tilde{w}(n)$.

The desired data, $r(n)$, can be expressed as:

$$\begin{aligned}r(n) &\triangleq r(nT_s) \\ &= r\left(nT_s + e(n) - e(n)\right) \\ &\approx r(nT_s + e(n)) - e(n)\dot{r}(nT_s + e(n)) \\ &= \tilde{r}(n) - e(n)\dot{r}(nT_s + e(n))\end{aligned} \tag{22}$$

where $\tilde{r}(n)$ are the distorted samples, $e(n)$ are the estimated sampling errors (see (7)), and $\dot{r}(nT_s + e(n))$ are the derivatives of $r(t)$ at $t = nT_s + e(n)$. The derivatives can be approximated using a discrete filter applied to $\tilde{r}(n)$. A block diagram showing the de-jittering process is illustrated in Figure 4.

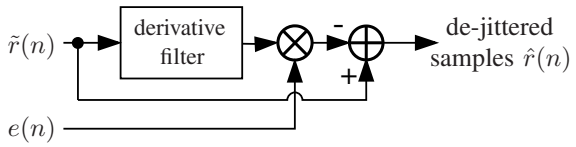

Fig. 4. Block diagram of the sideband suppression scheme.

In [11], the sampling offsets $e(n)$ are random and are estimated from $\tilde{w}(n)$ using a multiplication and filtering process. However, in the present situation, the same algorithm cannot estimate the offsets caused by the spurious PLL tones. This is because the sampling offsets (7) induced by the distorted PLL are much smaller compared to the scenario in [11]. In [11], the jitter errors are assumed to be in the range of 100ps. From (6) and (7), if the PLL sidebands power are at -50dBc from the desired clock signal, the sampling errors induced by the PLL sidebands are in the range of 1ps.

To solve this problem, we exploit the fact that the sampling offsets are parameterized by $\{C_0, \theta_0\}$ and the parameters can be estimated. This is represented by the "Parameter and Jitter Estimation" block in Figure 3. The steps in the algorithm are presented below. Each iteration represents a time period. Let $\{C_0, \theta_0\} = \{0, 0\}$.

Parameter and Jitter Estimation

In the k^{th} iteration,

1) Collect a sequence of $\tilde{w}(n)$ of length L, $n = (k-1)L+1 \rightarrow kL$.
2) Use (18) to estimate $\{C_k, \theta_k\}$ from the sequence.
3) Use (7) and $\{C_{k-1}, \theta_{k-1}\}$ to estimate the sampling offsets, $e(n)$, for the jitter compensation algorithm.

The distorted signal of interest $\tilde{r}(n)$ is obtained from the sampled data using a low-pass filter. From Figure 3, the jitter compensation algorithm uses the estimated sampling offsets $e(n)$ and the filtered signal $\tilde{r}(n)$ to generate the de-jittered samples $\hat{r}(n)$.

Figure 5 shows a realization where two sinusoidal signals at frequencies of 100MHz and 200MHz are used as the input signal, $r(t)$, into the ADC. Due to the distortions in the PLL clock, spurious tones appear on both sides of each input tone. This is shown in the left plot of Figure 5. The right plot of Figure 5 shows the reduction of the spurious tones using the proposed architecture.

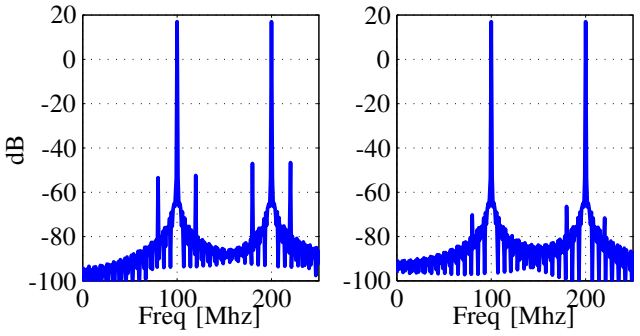

Fig. 5. The left figure shows the PSD of the sampled data. The right figure shows the PSD of the compensated signals using the proposed architerture.

The proposed method is tested over a range of input frequencies in simulation. The frequency of the sampling clock, low-frequency sinusoidal signal and the high-frequency sinusoidal signal are $f_s = 1$GHz, $f_w = 40$MHz and $f_y = 420$MHz, respectively. The high frequency signal includes a noise bandwidth of 5MHz. The frequency of the reference signal in the PLL feedback loop is $f_{\text{ref}} = 20$MHz. The input signal used is a sinusoidal tone whose frequency is varied from 25MHz to 250MHz in steps of 25MHz. In the parameter estimation algorithm, a sequence of $\tilde{w}(n)$ of length L is used to estimate $\{C_k, \theta_k\}$ (18). Three different sequence lengths are used in the simulations and they are $2^{18}, 2^{19}$ and 2^{20}.

Figure 6 shows the average results over 100 simulation runs. The plot shows the relative power of the spurious sidebands to the power of the input tone (dBc) over different frequencies, before and after using the proposed method. It is observed that the sidebands are reduced by more than 20dB when a sequence length of 2^{20} is used.

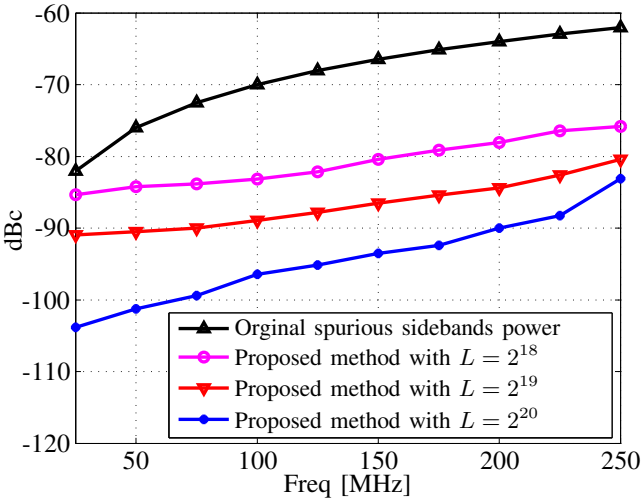

Fig. 6. A sinusoidal input is sampled using the distorted PLL clock. The plot shows the relative power of the spurious sidebands (in the sampled data) to the power of the input tone before and after compensation. The value L represents the length of the sequence that is used in the parameter estimation algorithm.

References

[1] T.-C. Lee and W.-L. Lee, "A spur suppression technique for phase-locked frequency synthesizers," in *Digest of Technical Papers, Proc ISSCC*, Feb. 2006, pp. 2432–2441.

[2] K.J. Wang, A. Swaminathan, and I. Galton, "Spurious tone suppression techniques applied to a wide-bandwidth 2.4 GHz Fractional-N PLL," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2787–2797, Dec. 2008.

[3] H. Wang, G. Shou, and N. Wu, "An adaptive frequency synthesizer architecture reducing reference sidebands," in *Proc. ISCAS*, Island of Kos, Greece, 2006, pp. 3081–3084.

[4] A. Tarighat, R. Bagheri, and A.H. Sayed, "Compensation schemes and performance analysis of IQ imbalances in OFDM receivers," *IEEE Transactions on Signal Processing*, vol. 53, no. 8, pp. 3257–3268, Aug. 2005.

[5] Q. Zou, A. Tarighat, and A.H. Sayed, "Joint compensation of IQ imbalance and phase noise in OFDM wireless systems," *IEEE Transactions on Communications*, vol. 57, no. 2, pp. 404–414, Feb. 2009.

[6] G.-C. Hsieh and J.C. Hung, "Phase-locked loop techniques: A survey," *IEEE Transactions on Industrial Electronics*, vol. 43, no. 6, pp. 609–615, Dec. 1996.

[7] R.E. Best, *Phase-Locked Loops, Design, Simulation, and Applications, 5th Edition*, McGraw-Hill, 2003.

[8] S. M. Kay, *Fundamentals of Statistical Signal Processing: Estimation Theory, Vol I.*, Prentice Hall, 1993.

[9] P. Stoica, R.L. Moses, B. Friedlander, and T. Soderstrom, "Maximum likelihood estimation of the parameters of multiple sinusoids from noisy measurements," *IEEE Transactions on Acoustics, Speech and Signal Processing*, vol. 37, no. 3, pp. 378–392, Mar 1989.

[10] M.D. Macleod, "Joint detection and high resolution ML estimation of multiple sinusoids in noise," in *Proc. ICASSP*, Salt Lake City, Utah, May 2001, vol. 5, pp. 3065–3068.

[11] Z.J. Towfic, S.-K. Ting, and A.H. Sayed, "Sampling clock jitter estimation and compensation in ADC circuits," in *Proc. ISCAS*, Pairs, France, May 2010.