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A NEW COMBINED ARCHITECTURE FOR CDMA LOCATION SEARCHERS AND RAKE RECEIVERS

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ABSTRACT

Location finding searchers have recently emerged as essential elements in future CDMA wireless systems. In this paper we present a new combined architecture for location searchers and conventional RAKE receivers, which is based on multiplexing common hardware blocks between the two structures. In so doing, most of the needed hardware for the conventional RAKE fingers and channel searcher is saved with no performance degradation. Furthermore, the new architecture can avoid the need to use delay locked loops.

1. INTRODUCTION

Wireless location finding has emerged as an essential public safety feature in future cellular systems. This feature has been mandated by a recent Federal Communications Commission (FCC) order that requires all wireless service providers to provide public safety answering points with information to locate an emergency 911 caller with an accuracy of 125 meters for 67% of the cases [1]. This has boosted research in the field of wireless location finding, with potential applications in areas such as location sensitive billing and fleet management (see, e.g., [2, 3, 4]).

Wireless location finding mainly requires accurate estimates of the time and amplitude of arrival of the first arriving ray of the mobile station signal when received at various base stations. Such estimates are obtained using a dedicated hardware block, which is conventionally termed *location searcher*. Several location searcher schemes have been developed in the past few years (see, e.g., [5]-[8]).

Another main hardware block in CDMA receivers is the conventional RAKE receiver, which consists of a dedicated channel searcher and a minimum of three RAKE fingers. Channel searchers obtain coarse estimates of the time and amplitude of arrival of the strongest multipath components of the mobile station signal. This information is then used by the receiver RAKE fingers and delay lock loops (DLLs) to lock onto the strongest channel multipath components, which are then combined and used in bit decoding. Estimates of the time and amplitude of arrival of the strongest rays are continuously fed from the channel searcher to the RAKE fingers.

Although the location searcher and RAKE receiver differ in purpose, structure, and estimation period, several basic building hardware blocks used in each of them are common. In this paper we exploit this fact to develop a new efficient combined hardware architecture for location searchers and RAKE receivers that serves to save several hardware blocks with added design flexibility and enhanced performance in many cases

2. CDMA LOCATION SEARCHERS AND RAKE RECEIVERS

Figure 1 shows a generic location searcher scheme for CDMA systems developed in [7, 8]. The scheme receives a sequence $\{r(n)\}_{n=1}^{K}$ that arises from the model:

$$r(n) = s(n) \star h(n) + v(n),$$

where $s(n) = [b(n) \cdot c(n)] \star p(n)$ is a real-valued CDMA sequence, which is formed by spreading a binary data sequence $b(n)$ using a code sequence $c(n)$, $p(n)$ is a known pulse shape impulse response sequence, $v(n)$ is additive white Gaussian noise, and $h(n)$ is a multipath channel that has the model

$$h(n) = \sum_{l=1}^{L} A_l x_l(n) \delta(n - \tau_l^o),$$

where A_l, $\{x_l(n)\}$, and τ_l^o are respectively the static amplitude, Rayleigh fading complex gain, and the time of arrival of the l^{th} multipath component (ray). The received sequence is used to estimate the discrete delay and amplitude of the prompt channel ray as follows. The received sequence $\{r(n)\}$ is despread by multiplying it by a replica of $\{s(n-\tau)\}$, for L_l different values of τ. The resulting sequence is first averaged coherently over an interval of N samples, and then averaged noncoherently for M samples to build a power delay profile. The averaging intervals N and M are positive integers that satisfy $K = NM$, and the value of N is picked adaptively in an optimal manner by using an estimate of the maximum Doppler frequency of the fading channel (f_D). The searcher then picks the earliest peak of the power delay profile and assigns its index to the time of arrival estimate. It also equalizes the peak value by subtracting two fading and noise biases, which are estimated by means of the upper and lower branches of the scheme of Figure 1. The output of this correction procedure is taken as an estimate for the amplitude of arrival. Further details of the operation of the scheme and its parameter choices are given in [7, 8].

On the other hand, RAKE receivers consist of L_c channel searcher branches and L_f RAKE fingers with three data branches in each finger. Each branch consists of a despreading stage followed by a noncoherent integration stage. The outputs of the searcher branches are processed to obtain coarse estimates of the time

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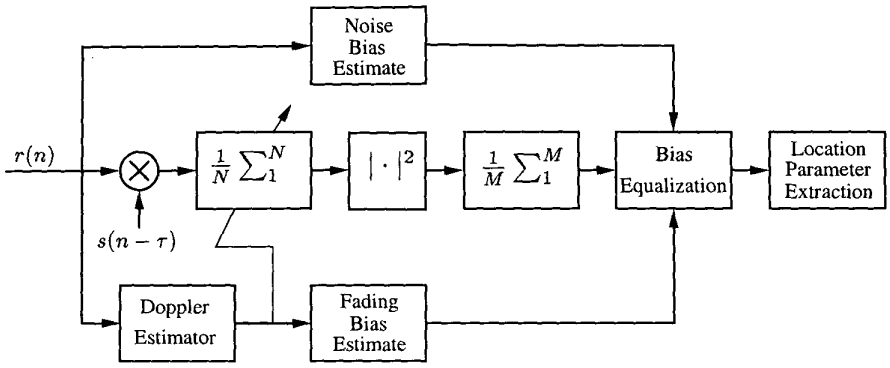

Figure 1: *A CDMA location searcher scheme.*

and amplitude of arrival of the strongest channel rays. The RAKE finger branches are then used to obtain finer estimates of the ray delays and amplitudes. Furthermore, channel rays are fine-tracked using delay locked loops (DLLs) [9].

The structure of CDMA RAKE receiver differs from the structure of the location searcher, shown in Figure 1, in the following aspects:

1. Channel fading can be assumed constant during the relatively short estimation period of the RAKE receiver, and is therefore totally ignored. On the other hand, location searchers use a much longer estimation period, which requires the searcher parameters to be adapted to an estimate of the channel maximum Doppler frequency [7, 8].

2. No fading or noise bias equalization is needed for the RAKE receiver as the fading and noise biases are negligible in this case [7, 8].

3. The received bits could be assumed to be known for the case of the location searcher as it usually uses frames of perfect cyclic redundancy check (CRC) or it can use the output decoded bits of the Viterbi decoder, which are at a high level of accuracy. This results in a delay of one frame period (20 ms for IS-95 systems). Such a delay is affordable for location searchers. However, channel searchers cannot afford such a delay and they apply the squaring process for each symbol to get rid of any bit ambiguity, which corresponds to N equal to the number of chips per symbol for the scheme in Figure 1. This requires a different coherent integration period for each searcher.

Despite these differences, we will propose a new combined hardware architecture for location searchers and RAKE receivers, which is based on exploiting the following two properties. First, the architectures of both structures have common building blocks such as correlators, squarers, and averaging registers. Second, the squaring and noncoherent averaging circuits of the location searcher are not used until the coherent average of N despread symbols is calculated. Thus we are able to develop a flexible multiplexed architecture for both searchers that saves most of the hardware blocks used for the RAKE receiver. This is done without no performance degradation in the performance of both systems. Furthermore, the combined architecture leads to enhancement of the performance of the RAKE receiver.

3. PROPOSED ARCHITECTURE

Figure 2 shows the scheme of the proposed combined architecture. The scheme is formed from L_l data branches. Each data branch starts with a correlator over N_1 samples (despreader), where N_1 is the number of chips per symbol multiplied by the number of data samples per chip (4, 8, or 16). The output of the correlator is then multiplexed between two paths, marked '1' and '2' in Figure 2. In path 1, which corresponds to data path of the channel searcher or RAKE finger branches, the despread signal is squared and noncoherently averaged over M_1 samples, where M_1 is *optionally* adapted to an estimate of the maximum Doppler frequency of the fading channel. For path 2, which is needed for the location parameter estimation, the despread sequence is delayed for a frame period, multiplied by an estimate of the transmitted bit sequence, coherently averaged over N_2 samples, squared, and noncoherently averaged over M_2 samples. Both N_2 and M_2 are adapted according to an estimate of the maximum Doppler frequency. The output of either paths is used to extract the channel multipath parameters.

The dynamic operation of the scheme is as follows. The received sequence is despread by multiplying by delayed code replica $c(n-\tau)$ and averaged over N_1 samples after which the N_1 register is reset. For online bit decoding, samples of the despread sequence are squared and noncoherently averaged. The average of every M_1 samples is passed to the multipath parameter extraction block and the M_1 register is then reset. Coarse multipath rays information are continuously fed to the L_f RAKE fingers, which use $3L_f$ branches of the scheme. to obtain *early, on-time and late* correlations over M_1 symbols. Such correlations are needed to advance or delay the sampling timing to lock onto the correct sampling point. This is done based on the difference between the early and late correlations [10]. The outputs of these fingers are combined, and used in bit decoding. Optional DLLs can be used to further enhance the tracking performance of the RAKE fingers. For location parameter estimation, the despread sequence is delayed, multiplied by an estimate of the transmitted bit sequence $\hat{b}(n)$, and continuously averaged over N_2 symbols. Every N_2 symbols, the N_2 register is reset and its output is squared using the shared squaring circuits and averaged over M_2 samples. After the total location estimation period ($N_2 \times M_2$ symbols), the time and amplitude of arrival of the prompt ray are equalized for fading and noise biases and used to extract needed location parameters.

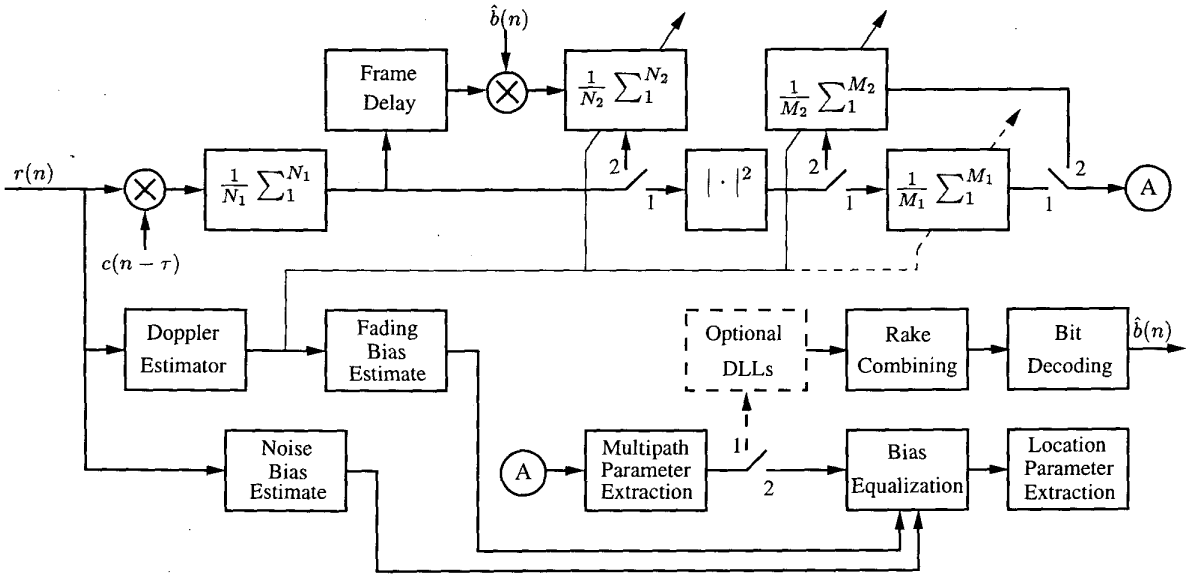

Figure 2: *Combined architecture for location searcher and RAKE receiver.*

4. SIMULATION RESULTS

The proposed architecture is simulated to investigate the accuracy of the time and amplitude of arrival estimates for both the RAKE receiver and location searcher. In the simulations a direct spread sequence is generated and filtered using a $T_c/8$ up-sampled IS-95 pulse-shaping filter, where T_c is the chipping period. The resulting signal is passed through a multipath Rayleigh fading channel of three resolvable rays and then white Gaussian noise, which accounts for both multiple access interference and thermal noise, is added. The received signal is sampled with a sampling period of $T_c/8$, then used to obtain estimates of the channel multipath delays and amplitudes. The search window used in the simulations is 20 chips wide and the carrier frequency f_c is 900 MHz. Each simulation point is the statistical average of 4000 runs.

Figures 3 and 4 show the mean absolute delay and the mean square amplitude estimation errors versus the chip energy-to-noise ratio (E_c/N_o) for both the RAKE channel searcher (CS) and the location searcher (LS) for various values of M_2. It is clear that the accuracy of the LS increases with M_2. However, this value is dictated by the duration the 911 caller stays online. We can also see that for M_2=128 and values of E_c/N_o higher than -40 dB, a mean absolute delay of 0.1 μsec and an amplitude MSE of -15 dB could be achieved. It was shown in a recent field trial that such an accuracy in fact meets the current FCC requirements for the case of resolvable multipath channels [11].

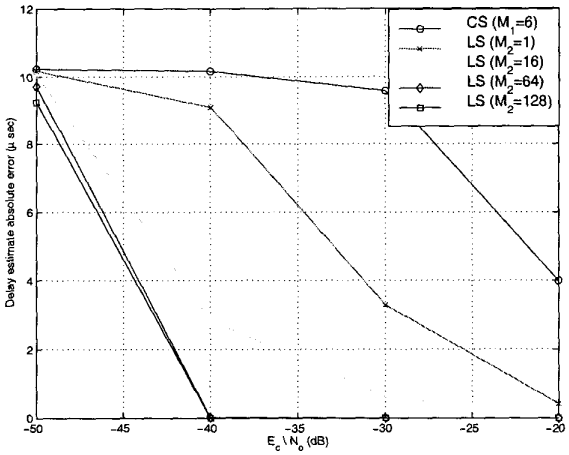

Figure 3: *Mean absolute delay estimation error versus E_c/N_o for $f_D = 10Hz$.*

5. HARDWARE COMPLEXITY REDUCTION

The proposed architecture has the following main advantages:

1. Saving a large number of hardware building blocks via multiplexing basic hardware blocks between 3 $L_f + L_c$ location searcher and RAKE receiver branches. This multiplexing saves a total number of gates equal to

$$(3\ L_f + L_c) \times (n_{bmult} + n_{sqr} + n_{reg}^{N_1} - 3\ n_{mux})\ ,$$

where n_{bmult}, n_{sqr}, n_{reg}^{N1}, and n_{mux} are the number of gates needed to implement a multiplier, squarer, register to store N_1 samples, and multiplexer, respectively. Figure 5(a) shows the percentage of the number of saved gates to the total number of gates of both the location searcher and RAKE receiver hardware versus the number of bits per sample (B), for the typical parameter values L_l=128, L_c=64, L_f=3, N_1=64, N_2=256, M_1=6, M_2=128 (see, e.g., [7, 11]). The figure shows that the proposed architecture can save up to 36% of the total number of gates. To further appreciate

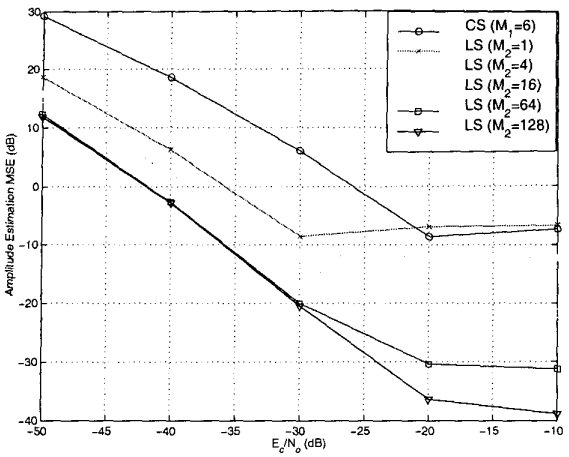

Figure 4: *Amplitude estimation MSE error versus E_c/N_o for $f_D = 40$ Hz.*

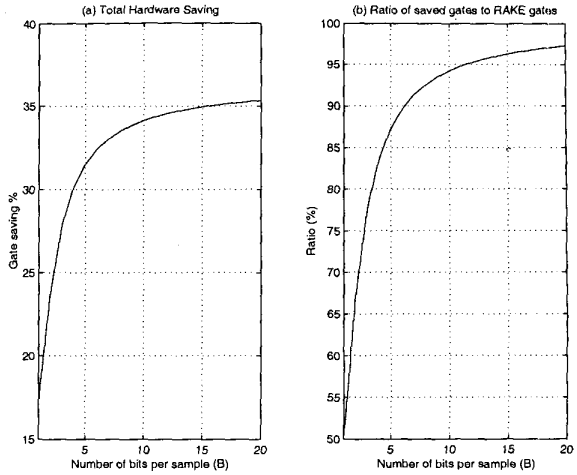

Figure 5: *Percentage of gate saving versus number of bits per sample. (a) Total. (b) RAKE.*

this amount of saved hardware, Figure 5(b) shows the ratio of the number of saved gates to the number of gates of the conventional RAKE receiver. This ratio can reach up to 96%. Here we assumed the use of carry-ripple adders and array multipliers [12].

2. Improving the performance of the RAKE receiver by continuously adapting the estimation period M_1 to an estimate of the maximum Doppler frequency. This period is conventionally adjusted to track a fading channel in the worst (fastest) case, which restricts this period to a small value (around 6 symbols for IS-95 systems). Adapting the estimation period of the channel searcher has two advantages. First, it will increase the accuracy of the delay and amplitude estimates. Second, it will help save power as it will reduce the number of times the RAKE fingers need to change their lock point, especially for low maximum Doppler frequency cases.

3. Reducing the hardware complexity significantly by eliminating the need to use DLLs for fine tracking in the cases where the accuracy of the used combined architecture is $T_c/8$ or higher (which is typical for location applications). In such cases the accuracy of the RAKE receiver will be adequate for online bit decoding without the use of DLLs. Hardware implementation of DLLs is extremely complex, especially with regard to the analog front end [10].

6. CONCLUSIONS

The paper presented a new combined architecture for CDMA location searchers and RAKE receivers. The new architecture is based on sharing common building blocks between the two structures. This leads to saving up to 36% of the total combined hardware, improving the RAKE receiver performance, and further reducing the hardware complexity by eliminating the need to use delay lock loops.

7. ACKNOWLEDGMENT

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