FREQUENCY DOMAIN COMPENSATION OF SPURIOUS SIDEBANDS IN A/D CIRCUITS

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ABSTRACT

In a non-ideal PLL circuit, leakage of the reference signal into the control line produces spurious tones. When the distorted PLL signal is used as a clock signal, it creates spurious tones in the sampled data. Our prior work used a training signal to estimate the distortions and then correct the samples. In this work, we propose an alternative approach that estimates and removes the distortions directly from the sampled data without a training signal. Simulations indicate that the proposed solution is able to reduce the root-mean-square (RMS) sampling errors to about 15% of the original values.

Index Terms— PLL, sideband suppression, spurious tones

1. INTRODUCTION

In the design of a phase-locked loop (PLL) frequency synthesizer, an important impairment is the presence of spurious tones. The spurious tones result from leakage of the reference signal into the control line of the voltage-controlled oscillator (VCO). When the sampling clock with spurious tones is used in the analog-to-digital converter (ADC), spurious sidebands are introduced into the sampled data. In applications such as spectrum sensing in cognitive radios, spurious tones from primary signals might give a false positive detection on free channels. Moreover, for wideband signals, the spurious sidebands are introduced directly into the frequency bands of the signals, thus reducing the signal-to-noise ratio (SNR).

There are two broad approaches to address the spurious tones problem. One approach is to reduce the spurious tones in the sampling clock by improving the PLL circuitry and the other approach is to correct the distortions by operating directly on the samples in the digital domain. In the circuit domain, the first approach attempts to improve the PLL circuit components, for example, by replacing the charge pumps (CP) with ones that have better linearity properties or using larger capacitors in the loop filter. More advanced solutions include making changes to the conventional design. For example, reference [1] proposed using multiple phase-frequency detectors (PFD) and CP that operate in delay with respect to one another. By operating in delay, the magnitude of the spurs is reduced, and the offset frequency is shifted further away from the clock frequency. Reference [2] proposed adding another tuning loop into the circuit design. The main tuning loop was used to lock to the PLL frequency synthesizer, and the second loop was activated when the first loop was locked. The second loop was used specifically for reducing the reference sidebands.

There are various proposed solutions to correct ADC distortions using digital processing techniques as well; typically, the approaches use some calibration signals or exploit some known effects. For example, reference [3] used a reference tone signal to reduce the jitters in narrowband signals. References [4–6] modified the approach and applied it to OFDM signals and general bandpass signals. Reference [7] proposed a technique that shifted a training signal into a suitable empty frequency band for jitter estimation. Then, the samples were compensated using the estimated jitter and a derivative filter. Reference [8] examined the effects of non-linearity in the track and hold circuitry and proposed a compact model to minimize the digital post-processing complexity; the parameters in the model were estimated using calibration signals. Reference [9] studied the signal dependent distortions due to the switches in the ADC using the Volterra series expansion.

Our previous work on reducing the effects of PLL sideband distortions was described in [10]. The work used a training signal (with a known frequency), which we used to estimate the distortions and then compensate the sampled data. In this paper, we propose an alternative algorithm that does not rely on the use of a training signal. Instead, the solution reduces the effect of the sampling jitters in the frequency domain directly.

2. EFFECTS OF LEAKAGE ON CLOCK SIGNAL

In [11, 12], a VCO is described as a circuit that generates a periodic clock signal, $s(t)$, whose frequency is a linear function of a control voltage, V_{cont}. Let the gain of the VCO and its "free running" frequency be denoted by K_{vco} and f_s, respectively. The generated clock signal is described by

$$s(t) = A_s \sin\left(2\pi f_s t + K_{\text{vco}} \int_{-\infty}^{t} V_{\text{cont}} dt\right) \tag{1}$$

To attain some desired oscillation frequency, V_{cont} is set to some constant value. However, the generated signal, $s(t)$, may not be an accurate tone. To attain good frequency synthesis, a down-converted version of the clock signal is fed into a block that consists of a phase-frequency detector (PFD), a charge pump (CP) and a low-pass filter (LPF) as shown in Figure 1. The PFD/CP/LPF block compares the

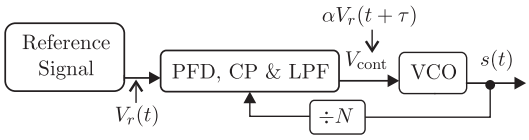

Fig. 1. Block diagram of a PLL.

down-converted frequency clock signal with a low-frequency reference signal at f_{ref} and makes adjustments to V_{cont}. Due to imperfections in the circuitry, the reference signal leaks into the control

This work was supported in part by DARPA contract N66001-09-1-2029. Authors' emails{tshangke,sayed}@ee.ucla.edu

line of the VCO. For simplicity, we assume that the desired clock signal is f_s and, hence, V_{cont} is 0. The reference signal is assumed to be some periodic signal with fundamental frequency f_{ref} [13]. A periodic signal can be described by its Fourier series representation. For illustration purposes, we assume here that the periodic signal is a sawtooth waveform whose Fourier series representation is

$$V_r(t) = \frac{2}{\pi}\sum_{k=1}^{\infty}\frac{1}{k}\sin(2\pi k f_{\text{ref}} t) \tag{2}$$

Now, suppose there is leakage and V_{cont} is

$$V_{\text{cont}} = \sum_{k=1}^{\infty} V_k \cos\left(2\pi f_k t + \theta_k\right) \tag{3}$$

where

$$\theta_k = 2\pi k f_{\text{ref}}\tau - \frac{\pi}{2}, \quad V_k = \frac{1}{k}V_0, \quad f_k = k f_{\text{ref}} \tag{4}$$

for some $\{V_0, \tau\}$. Then the output of the VCO becomes

$$s(t) = A_s \sin\left(2\pi f_s t + \sum_{k=1}^{\infty} C_k \sin\left(2\pi f_k t + \theta_k\right)\right) \tag{5}$$

Using a first order approximation in (5), some analysis gives $s(t)$ as

$$\begin{aligned} s(t) \approx A_s \sin(2\pi f_s t) + \sum_{k=1}^{\infty}\frac{A_s C_k}{2}\left[\sin(2\pi(f_s + f_k)t + \theta_k)\right. \\ \left. - \sin(2\pi(f_s - f_k)t - \theta_k)\right] \end{aligned} \tag{6}$$

This expansion shows that the distorted sampling clock signal contains multiple sidebands at $f_s \pm f_k$. Now the actual sampling instants of an ADC that uses a clock signal of the form of (5) are the zero-crossings of $s(t)$. Using (5) and defining $T_s = 1/f_s$, the sampling instants, t_n, of the ADC must satisfy the condition:

$$t_n + \sum_{k=1}^{\infty}\frac{C_k}{2\pi f_s}\sin\left(2\pi f_k t_n + \theta_k\right) = nT_s \tag{7}$$

Some Taylor series analysis will show that the zero-crossings occur at times $t_n = nT_s + e(n)$, where

$$e(n) \approx -\sum_{k=1}^{\infty}\frac{C_k}{2\pi f_s}\sin\left(2\pi f_k n T_s + \theta_k\right) \tag{8}$$

We omit the derivation for brevity. Let us analyze the effect of this distorted sampling on the input signal. Let the input signal to the ADC be $r(t)$. Then the sampled signal, $\check{r}(n)$, is approximated as

$$\begin{aligned} \check{r}(n) &\approx r\left(nT_s + e(n)\right) \\ &\approx r(n) + e(n)\,\dot{r}(n) \end{aligned} \tag{9}$$

where $r(n) = r(t)|_{t=nT_s}$ and $\dot{r}(n) = \dot{r}(t)|_{t=nT_s}$. Note that $e(n)$ in (8) consists of a summation of frequency tones at f_k. Thus, the term $e(n)\,\dot{r}(n)$ in (9) can be interpreted as replicas of $\dot{r}(n)$ that are multiplied and frequency-shifted to $f_r \pm f_k$, where f_r is the center frequency of $r(t)$. If the Fourier series coefficients of the reference signal in the PLL decrease rapidly, then the higher frequency components in (8) and $e(n)\,\dot{r}(n)$ can be ignored.

As an example, the reference signal is simulated as a sawtooth wave with f_{fref} of 20MHz and is approximated using the first 8 Fourier series coefficients. The coefficient C_0 is set to 6.32×10^{-3}, which implies that the power ratio of the sideband at $f_s + f_1$ of the clock, $s(t)$, to the tone at f_s is -50dBc. An input tone signal is sampled with offsets $e(n)$ in (8) and its power spectral density (PSD) is shown in Fig. 2. The left and right plots show the effects on the tone when it is at 100MHz and 400MHz, respectively.

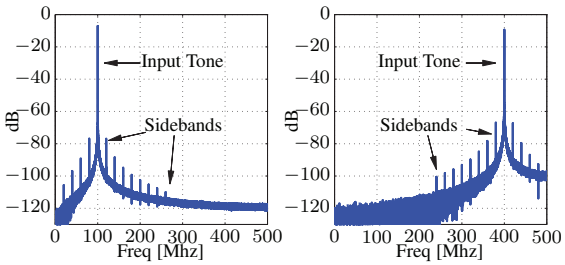

Fig. 2. The left and right plots show the PSD of the distorted tone at 100MHz and 400MHz.

3. PROPOSED SOLUTION

First, we review the compensation method used in our previous works [7, 10] to dejitter the sampled data. This formulation serves as a motivation to derive our proposed algorithm in this paper.

3.1. Jitter Compensation

The desired data, $r(n)$, can be expressed as:

$$\begin{aligned} r(n) &\triangleq r(nT_s) \\ &= r\left(nT_s + e(n) - e(n)\right) \\ &\approx r(nT_s + e(n)) - e(n)\dot{r}(nT_s + e(n)) \\ &= \check{r}(n) - e(n)\dot{\check{r}}(n) \end{aligned} \tag{10}$$

where $\check{r}(n)$ are the distorted samples, $e(n)$ are the sampling errors to be estimated, and $\dot{\check{r}}(n)$ are the derivatives of $r(t)$ at $t = nT_s + e(n)$. The derivatives can be approximated using a discrete filter applied to $\check{r}(n)$. In this paper, a 15-tap filter is derived using the technique proposed in [14]. The frequency response is shown in Fig. 3.

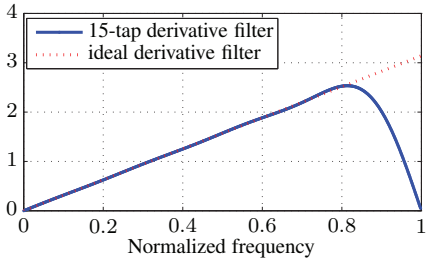

Fig. 3. The plot shows the frequency response of the derivative filter.

3.2. Jitter Estimation

From (9), it is seen that $e(n)$ creates spurious frequency components at multiples of f_{ref} away from the input signal. We would like to use (10) to remove the spurious frequency components (see Fig. 2). It is reasonable to assume that we can detect some strong frequency components in the input signal, for example, by examining the frequency content of a segment of the data. Then, we know from the previous analysis (9) that there are spurious frequency components at multiples of f_{ref} away from these detected frequency components. The objective is to remove these spurious tones after compensation. We assume that it is only important to remove up to the Mth spurious

frequency components, and we express the optimization problem using (10) as

$$\min_{\boldsymbol{e}} \|F(\boldsymbol{r} - D\boldsymbol{e})\|^2 \tag{11}$$

where F is a Discrete Fourier Transform (DFT) submatrix of size N by L, which corresponds to the frequency regions/bins where the spurious frequency components lie; $\boldsymbol{r}$ is a vector of size L and its nth element is $\check{r}(n)$; D is a diagonal matrix of size $L \times L$ and $D(n,n)$ is $\dot{\check{r}}(n)$. $\boldsymbol{e}$ is a vector of $e(n)$ that are to be estimated. The optimization problem finds an $\hat{\boldsymbol{e}}$ that minimizes the frequency components in the regions defined by F.

We also exploit the fact that $e(n)$ has frequency components at multiples of f_{ref} (see (8)). Recall that in (11), we assume it is sufficient (or it is only important) to remove up to the Mth spurious frequency components. Therefore, we express $\boldsymbol{e}$ as

$$\boldsymbol{e} \approx G\boldsymbol{h} \tag{12}$$

where $G = [S_1\, C_1\, \ldots\, S_M\, C_M]$, S_k and C_k, $k = 1, \ldots, M$, are vectors of size L and their nth elements are $\sin(2\pi f_k n T_s)$ and $\cos(2\pi f_k n T_s)$, respectively. Finally, $\boldsymbol{h}$ is to be estimated. Note that the size of $\boldsymbol{h}$ is $2M$. For example, in Fig. 2, we can detect the frequency bin where the strong signal lies in the frequency domain and generate matrix F with $N = 2MK$ rows that define $2M$ frequency regions on the left and right sides of the detected frequency. Each frequency region can be defined by K frequency bins. Therefore, (11) becomes

$$\min_{\boldsymbol{h}} \|F\boldsymbol{r} - FDG\boldsymbol{h}\|^2 \tag{13}$$

The above least squares problem has $2MK$ equations and $2M$ unknowns and a closed-form solution for $\hat{\boldsymbol{h}}$ can be obtained. Then, the estimated sampling offsets and the dejittered samples are $\hat{\boldsymbol{e}} = G\hat{\boldsymbol{h}}$ and $\boldsymbol{r} - D\hat{\boldsymbol{e}}$, respectively. A summary of the proposed algorithm is stated below.

Proposed Algorithm

1. Obtain $\dot{\check{r}}(n)$ using the derivative filter on $\check{r}(n)$.
2. Detect the strong frequency components in $\check{r}(n)$.
3. Create the matrices F, D and G.
4. Solve $\min_{\boldsymbol{h}} \|F\boldsymbol{r} - FDG\boldsymbol{h}\|^2$ to obtain $\hat{\boldsymbol{h}}$.
5. Obtain $\hat{\boldsymbol{e}}$ and $\hat{\boldsymbol{r}}$ from $\hat{\boldsymbol{e}} = G\hat{\boldsymbol{h}}$ and $\hat{\boldsymbol{r}} = \boldsymbol{r} - D\hat{\boldsymbol{e}}$.

4. SIMULATIONS RESULTS

Computer simulations are performed to analyze the performance of the algorithm. For illustration, we assume that the sampling frequency f_s of the ADC is 1GHz, and the reference signal is a sawtooth function (2) with a fundamental frequency f_{ref} of 20MHz. The sampling offsets $e(n)$ are generated using (8). C_0 is set to 6.32×10^{-3} so that the power ratio of the spurious sidebands at $f_s \pm f_{\text{ref}}$ to the signal at f_s is -50dB. The sawtooth function is truncated to the first 4 coefficients, which creates 8 sidebands that are multiples of f_{ref} away from the input signal. In the presence of noise, not all the sidebands are observable (see an example in Fig. 4 ahead). The input signal is a sinusoid signal that is varied from 100MHz to 400MHz. The amplitude of the tone is set to 0.9 and the data is quantized by assuming a 10bit ADC with an input range of ± 1. White Gaussian noise (WGN) with standard deviation of 5×10^{-4} is added into the input data before quantization. Other noise sources exist in a practical ADC as well. One example is the phase noise of the sampling clock that creates random time jitter in the sampled data. Thus, random time jitter based on a first order PLL model is also generated. The phase noise model is described in the appendix (at the end of the paper). For the phase noise model, the loop bandwidth f_L is set to 5MHz and the standard deviation of the random jitter (normalized to the sampling interval) is defined as σ_τ. The simulation results are averaged over 50 simulations runs.

Fig 4 shows a realization of a distorted sampled signal at 350MHz before and after using the proposed algorithm. Using

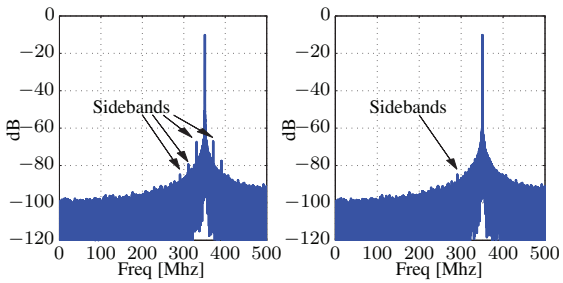

Fig. 4. The left and right plots show the PSD of a distorted tone before and after using the proposed algorithm, respectively.

the proposed algorithm, we choose to reduce the sidebands that are 20MHz and 40MHz away from the input signal. This implies that M=2 and 4 frequency regions on the left and right side of the input signal's frequency are used to generate the DFT submatrix F in (13). In each frequency region, $K = 5$ frequency bins are used.

For the first set of simulations, σ_τ is set to 0.01 and the length of the sampled data, L, is $\{2^{16}, 2^{17}, 2^{18}\}$. Fig. 5 shows the performance of the algorithm using two measures. The first measure is the sideband suppression performance using the proposed method. The left-sided plots in the figure show the suppression of the sidebands at 20MHz and 40MHz away from the input signal's frequency. It also shows the performance when L is varied. When $L = 2^{18}$, the average sideband suppression at 20MHz and 40MHz away from the input tone is 25dB and 16dB, respectively. The second measure is used to compare the estimation performance of $e(n)$. The RMS of the estimation error $(\hat{\boldsymbol{e}} - \boldsymbol{e})$ is divided by the RMS of the actual $\boldsymbol{e}$ to obtain a ratio of the estimation error. The right plot in the figure shows the ratio of the error as the input signal is varied across frequency and L. When $L = 2^{18}$ the average ratio is 0.15.

For the second set of simulations, L is set to 2^{18} and σ_τ is chosen from the set $\{0.001, 0.01, 0.1\}$. Fig. 6 shows the performance of the algorithm using the same measures. The left-sided plots in the figure show the suppression of the sidebands at 20MHz and 40MHz away from the input signal's frequency at the various σ_τ. When σ_τ is between 0.001 to 0.01, the average sideband suppression at 20MHz and 40MHz away from the input tone is 27dB and 18dB, respectively. The right-sided plot in the figure shows the ratio of the estimation error across input frequency and σ_τ. When σ_τ is between 0.001 to 0.01, the average ratio is 0.14.

5. CONCLUSION

We proposed an algorithm to mitigate the spurious sideband distortions caused by the PLL clock. The approach exploits the fact the distortions occur at multiples of the reference frequency f_{ref} from the

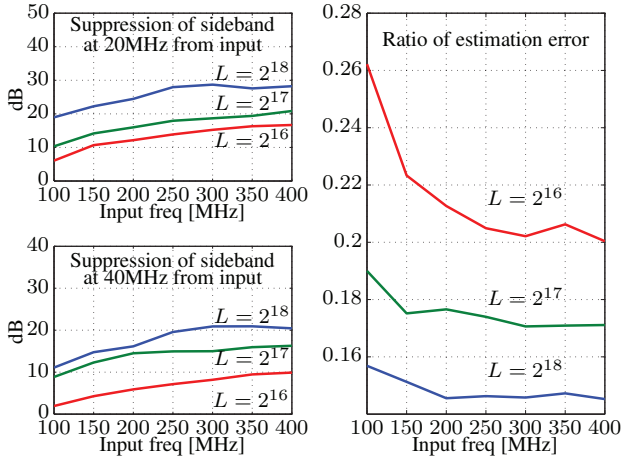

Fig. 5. The left and right plots show the algorithm performance in terms of sideband suppression and estimation error when L is varied.

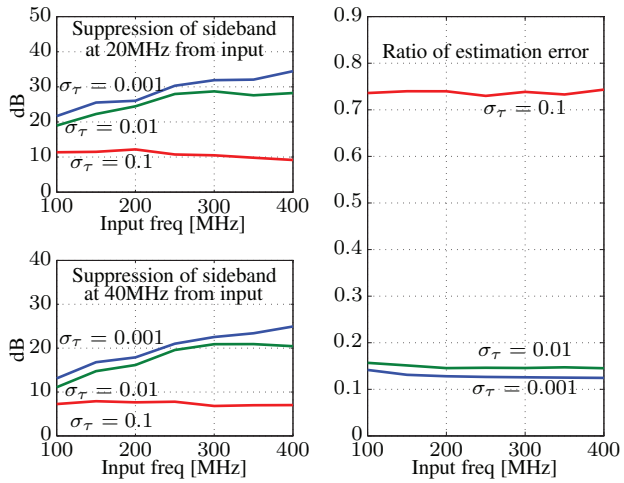

Fig. 6. The left and right plots show the algorithm performance in terms of sideband suppression and estimation error when σ_τ is varied.

center frequency of the input signal and finds a solution that minimize these effects. The simulations show that the proposed solution is able to reduce the sideband distortions in the presence of various noises, including WGN, quantization noise and PLL phase noise. Under the simulation parameters, the RMS sampling offsets are reduced to 0.15 of the original sampling offsets and the sidebands at 20MHz and 40MHz from the center frequency of the input signal are reduced by 25dB and 16dB.

6. APPENDIX: PHASE NOISE IN FIRST ORDER PLL

From [15], the single-sided PSD of the phase noise model for the first-order PLL is

$$S_\phi(f) = \frac{\nu}{\pi(f^2 + f_L^2)} \tag{14}$$

where f_L is a measure of the loop bandwidth and ν is called the oscillator linewidth. The variance is $\frac{\nu}{2f_L}$ and the autocorrelation function of the phase noise $\phi(t)$ is

$$R_\phi(\lambda) = \int_{-\infty}^{\infty} \frac{\nu}{2\pi(f^2 + f_L^2)} df \tag{15}$$

Therefore, we can relate the phase noise to the time jitter in a clock signal with frequency f_s as $\phi(t) = 2\pi f_s \tau(t)$. The standard deviation of the random jitter is $\frac{1}{2\pi f_s}\sigma_\phi$. Normalizing the standard deviation to the sampling interval yields $\sigma_\tau = \frac{1}{2\pi}\sigma_\phi$.

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